

REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 1 and 2 are pending in this application. Claims 1 and 2 were rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent Application Publication 2004/0207593 to Ha et al. (herein "Ha"). Claims 1 and 2 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent Application Publication 2003/0107544 A1 to Edwards. Those rejections are traversed by the present response as discussed next.

Independent claim 1 is directed to an array substrate for a flat display device. With reference to Figure 2 in the present specification as a non-limiting example, a plurality of switches ASW1-ASWn are placed between output lines D1-Dx and signal lines S1-Sn. Further, switch control signal lines ASWL1, ASWL2 supply control electrodes of the switches ASW1-ASWn with control signals.

As also shown in Figure 2, a plurality of electrode patterns P1-Pn connect the control electrode of each switch ASW1-ASWn to any one of the switch control signal lines ASWL1, ASWL2, and further the electrode patterns P1-Pn each two-dimensionally overlap all of the switch control signal lines ASWL1, ASWL2, and have substantially identical shapes.

Figure 3 shows a comparison device with respect to Figure 2 in which electrode patterns do not overlap each of switch control signal lines and do not have substantially identical shapes. As recognized by the applicants of the present invention, in such a device as in Figure 3, with the shape of such electrode patterns not overlapping all of the switch control signal lines and not having substantially identical shapes, parasitic capacitances of left and right switches ASW may be unequal.¹

The present inventors recognized that the claimed structure, and again with reference to Figure 2 in the present specification as a non-limiting example, in which the electrode

¹ Specification at page 10, lines 15-24.

patterns P1-Pn overlap all of the switch control signal lines ASWL1, ASWL2, and which all have substantially identical shapes, can provide significant benefits. First, all of the left and right switches will have approximately equal parasitic capacitances, thereby times required to charge adjacent pixels with data signals are approximately equal, and thereby display unevenness is eliminated and favorable display characteristics can be obtained.² Further, with the claimed electrode configuration, differences in lengths between the electrode patterns P1-Pn can be easily found by visual inspection, and thereby process yield can be improved.³ Further, with the claimed structure it is only necessary to change a contact hold formation layer to change the connection between the electrode patterns and the appropriate control signal line ASWL1, ASWL2, and thereby there is no need to change a plurality of masks, and costs as a result of design changes can be reduced, in addition to providing more flexibility in circuit design.⁴

Applicants respectfully submit the above-noted features particularly directed to the “plurality of electrode patterns” are neither taught nor suggested by either of the applied art to Ha or Edwards. More specifically, applicants respectfully submit neither Ha nor Edwards disclose or suggest the above-noted features that:

wherein the electrode patterns each two-dimensionally overlap *all* of the switch control signal lines and have *substantially identical* shapes. [Emphasis added].

First with respect to Ha, the outstanding Office Action merely references paragraph [0014] in Ha with respect to the above-noted claim features. However, that paragraph in its entirety states:

[0014] The gate shift register 16 shifts control signals (start pulses) applied by the control chip 22 to sequentially apply gate pulses to the gate lines GL.

² Specification at page 10, line 25 to page 11, line 3.

³ Specification at page 11, lines 4-8.

⁴ Specification at page 11, lines 9-18.

Applicants submit clearly that disclosure in Ha is completely irrelevant to the above-noted claimed features that “the electrode patterns each two-dimensionally overlap all of the switch control signal lines and have substantially identical shapes”. Ha merely discloses a circuit diagram indicating connections between the control electrodes of switches S and switch control signal lines C, see for example Figures 2 and 18.

Applicants also further note the grounds for the rejection based on Ha has not even indicated what elements in Ha correspond to the “plurality of electrode patterns”.

In view of the foregoing comments applicants respectfully submit Ha clearly does not disclose or suggest the above-noted claim features directed to the “electrode patterns”.

With respect to Edwards, applicants note the grounds for the outstanding rejection first does not indicate any disclosure in Edwards directed to the above-noted claim features that “the electrode patterns each two-dimensionally overlap all of the switch control signal lines and have substantially identical shapes”. For that reason alone the outstanding rejection based on Edwards is traversed.

Moreover, applicants submit the outstanding grounds for rejection does not even clearly indicate what elements in Edwards are relied upon to correspond to “a plurality of electrode patterns”. Edwards does not appear to disclose any such elements for example in cited Figures 1 or 2, and particularly Edwards does not appear to disclose any elements that connect control electrodes of each switch to switch control signal lines. For such further reasons the outstanding rejection based on Edwards is traversed.

In view of the foregoing comments applicants respectfully submit the claims as currently written clearly distinguish over both Ha and Edwards.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

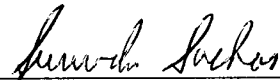
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